Academic Course Description

BHARATH UNIVERSITY
Faculty of Engineering and Technology
Department of Electronics and Communication Engineering

BEC302 Principles of Digital Electronics

Third Semester, 2017-18 (Odd Semester)

Course (catalog) description

The purpose of this course is to develop a strong foundation in analysis and design of digital electronics. This course introduces combinational and sequential circuit design. It also discussed concepts of memory, programmable logic and digital integrated circuits. Upon completion, students should be able to construct, analyze, verify, and troubleshoot digital circuits using appropriate techniques and test equipment

Compulsory/Elective course **:** Compulsory for ECE students

Credit & contact hours : 4 & 60

Course Coordinator : Dr M.Sangeetha, Professor

Instructors **:**

Name of the instructor	Class handling	Office location	Office phone	Email (domain:@ bharathuniv.ac.in	Consultation
Dr M.Sangeetha	Second year ECE	SA block		sang_gok@yahoo.com	9.00 - 9.50 AM
Dr. Karthik	Second year ECE	SA block		karthik.ece@bharathuniv.ac.in	12.45 - 1.15 PM

Relationship to other courses:

Pre –requisites **:** BEE101 Basic Electrical & Electronics Engineering

Assumed knowledge : Basic knowledge in Logic gates and Transistors

Following courses : BEC502 Microprocessors and Microcontroller, BEC702 DIGITAL CMOS VLSI

Syllabus Contents

UNIT I BASIC CONCEPTS ,BOOLEAN ALGEBRA AND LOGIC GATES **12 HOURS**

Number systems - Binary, Octal, Decimal, Hexadecimal, conversion from one to another, complement arithmetic, Boolean theorems of Boolean algebra, Sum of products and product of sums, Minterms and Maxterms, Karnaugh map, Quine-McCluskeymethodofminimization .NAND-NOR implementation of Logic gates,Multilevel gate implementation,Multi output gate implementation,TTL and CMOS logic and their characteristics,Tristate gates.

UNIT II COMBINATIONAL CIRCUITS **12 HOURS**

Problem formulation and design of combinational circuits, Half Adder ,Full adder,HalfSubtractor, Full Subtractor, Carry Look Ahead adder, BCD adder, Fast adder,Serial adder/subtractor,BinaryMultiplier,Binary Divider, Encoder ,Decoder, Mux / Demux, Code-converters, Parity Generators, Comparators.

UNIT III SEQUENTIAL CIRCUIT **12 HOURS**

Latches,Flipflops - SR, JK, T, D, Master/Slave FF, Triggering of FF,Realization of one flip flop using other flip flops Analysis of clocked sequential circuits - their design, State minimization, State assignment, Circuit implementation, Registers-Shift registers, Asynchronous Up/Downcounter SynchronousUp/Down counters, Modulo–ncounter, Ring counter ,Shift counters ,Sequence generators.

UNIT IV MEMORY DEVICES **12 HOURS**

Classification of memories – ROM ,ROM organization - PROM , EPROM ,EEPROM , EAPROM, RAM – RAM organization – Write operation , Read operation , Memory cycle, Timing wave forms , Memory decoding , memory expansion , Static RAM Cell, Dynamic RAM cell ,Programmable Logic Devices – Programmable Logic Array (PLA) and Programmable Array Logic (PAL) ,Field Programmable Gate Arrays (FPGA) ,Implementation using ROM, PLA, and PAL.

UNIT V SYNCHRONOUS AND ASYNCHRONOUS SEQUENTIAL CIRCUITS **12 HOURS**

Synchronous Sequential Circuits: General Model – Classification – Design – Use ofAlgorithmic State Machine – Analysis of Synchronous Sequential Circuits.
Asynchronous Sequential Circuits: Design of fundamental mode and pulse mode circuits – Incompletely specified State Machines – Problems in Asynchronous Circuits – Design of Hazard Free Switching circuits.

Total : 60 HOURS

Text book(s) and/or required materials

T1. M. Morris Mano, “Digital Design”, 4th Edition, Prentice Hall of India Pvt. Ltd., 2008 / Pearson Education (Singapore) Pvt. Ltd., New Delhi, 2003.

T2. William I. Fletcher, " An Engineering Approach to Digital Design ", Prentice-Hall of India, 1980.

Reference Books:

R1. John F.Wakerly, “Digital Design”, Fourth Edition, Pearson/PHI, 2008

R2 John.M Yarbrough, “Digital Logic Applications and Design”, Thomson Learning,2006.

R3. Charles H.Roth. “Fundamentals of Logic Design”, 6th Edition, Thomson Learning, 2013.

R4. Donald P.Leach and Albert Paul Malvino, “Digital Principles and Applications”, 6th Edition,TMH,2006.

R5. http://www.electrical4u.com/digital-electronics

Computer usage: EDA tools like ORCAD SPICE,Logisim

Professional component

General	-	0%
Basic Sciences	-	0%
Engineering sciences & Technical arts	-	0%
Professional subject	-	100%

Broad area : Communication| Signal Processing**| Electronics** | **VLSI**| Embedded

Test Schedule

S. No.	Test	Tentative Date	Portions	Duration
1	Cycle Test-1	August 1st week	Session 1 to 14	2 Periods
2	Cycle Test-2	September 2nd week	Session 15 to 28	2 Periods
3	Model Test	October 2nd week	Session 1 to 45	3 Hrs
4	University Examination	TBA	All sessions / Units	3 Hrs.

Mapping of Instructional Objectives with Program Outcome

This course is to develop a strong foundation in analysis and design of digital electronics. This course introduces combinational and sequential circuit design. It also discussed concepts of memory, programmable logic and digital integrated circuits.	Correlates to program outcome		
	H	**M**	**L**
1. Recall the different number systems and demonstrate the simplification of Boolean expressions using Boolean algebra & K-Map method.	a,b,d	f,i	e
2. Analyze the Combinational building blocks	b,d	a,c,f	
3. Analyze the sequential building blocks	a,b		
4. Develop a state diagram and simplify the given sequential logic.	a		
5. To illustrate the concept of synchronous sequential circuits	b,d	a,c,f,i	
6. To illustrate the concept of asynchronous sequential circuits	a,b,d	c,i	

H: high correlation, M: medium correlation, L: low correlation

Draft Lecture Schedule

S.NO	Topics	Problem solving (Yes/No)	Text / Chapter
UNIT I	**BASIC CONCEPTS ,BOOLEAN ALGEBRA AND LOGIC GATES**		
1.	Number systems - Binary, Octal, Decimal, Hexadecimal, conversion from one to another	Yes	[T1] Chapter -1,2,3,10 [R3]Chapter-6, 7
2.	complement arithmetic	Yes	
3.	Boolean theorems of Boolean algebra, Sum of products	Yes	
4.	Product of sums, Minterms and Maxterms	Yes	
5.	Karnaugh map	Yes	
6.	Quine-McCluskeymethod	Yes	
7.	NAND-NOR implementation of Logic gates,Multilevel gate implementation	Yes	
8.	Multi output gate implementation	Yes	
9.	TTL and CMOS logic and their characteristics,Tristate gates	No	
UNIT II	**COMBINATIONAL CIRCUITS**		
10.	Problem formulation and design of combinational circuits	No	[T1] Chapter -4, [R1]Chapter-9,11
11.	Half Adder ,Full adder, Half Subtractor, Full Subtractor	Yes	
12.	Carry Look Ahead adder	Yes	
13.	BCD adder, Fast adder	Yes	
14.	Serial adder/subtractor	Yes	
15.	BinaryMultiplier, Binary Divider	Yes	
16.	Encoder ,Decoder, Mux / Demux	Yes	
17.	Code-converters	Yes	
18.	Parity Generators, Comparators	Yes	
UNIT III	**SEQUENTIAL CIRCUIT**		
19.	Latches,Flipflops - SR, JK, T, D	Yes	[T1] Chapter -5,6 [R1]Chapter-4
20.	Master/Slave FF, Triggering of FF	Yes	
21.	Realization of one flip flop using other flip flops	Yes	
22.	Analysis of clocked sequential circuits - their design	Yes	
23.	State minimization, State assignment, Circuit implementation	Yes	
24.	Registers-Shift registers	No	
25.	Asynchronous Up/Downcounter	Yes	
26.	SynchronousUp/Down counters	Yes	
27.	Modulo–ncounter, Ring counter	Yes	
28.	Shift counters ,Sequence generators	Yes	
UNIT IV	**MEMORY DEVICES**		
29.	Classification of memories – ROM	No	
30.	ROM organization - PROM , EPROM ,EEPROM , EAPROM	No	
31.	RAM – RAM organization – Write operation , Read operation	No	

32.	Memory cycle, Timing wave forms	No	[T1] Chapter – 7, [R1]Chapter-7
33.	decoding , memory expansion	No	
34.	Static RAM Cell, Dynamic RAM cell	No	
35.	Programmable Logic Devices – Programmable Logic Array (PLA)	Yes	
36.	Programmable Array Logic (PAL)	No	
37.	Field Programmable Gate Arrays (FPGA)	No	
38.	Implementation using ROM, PLA, and PAL.	Yes	
UNIT V	**SYNCHRONOUS AND ASYNCHRONOUS SEQUENTIAL CIRCUITS**		
39.	General Model – Classification – Design – Use ofAlgorithmic State Machine	Yes	[T1] Chapter -8, 9 [R1]Chapter-12,14
40.	Analysis of Synchronous Sequential Circuits	Yes	
41.	Design of fundamental mode	Yes	
42.	Design of pulse mode circuits	Yes	
43.	Incompletely specified State Machines	Yes	
44.	Problems in Asynchronous Circuits	Yes	
45.	Design of Hazard Free Switching circuits.	Yes	

Teaching Strategies

The teaching in this course aims at establishing a good fundamental understanding of the areas covered using:

- Formal face-to-face lectures
- Tutorials, which allow for exercises in problem solving and allow time for students to resolve problems in understanding of lecture material.
- Laboratory sessions, which support the formal lecture material and also provide the student with practical construction, measurement and debugging skills.
- Small periodic quizzes, to enable you to assess your understanding of the concepts.

Evaluation Strategies

Cycle Test – I	-	5%
Cycle Test – II	-	5%
Model Test	-	10%
Assignments/Seminar/online test/quiz	-	5%
Attendance	-	5%
Final exam	-	70%

Prepared by: Dr M.Sangeetha Professor , Department of ECE **Dated :**

Addendum

ABET Outcomes expected of graduates of B.Tech / ECE / program by the time that they graduate:

a) An ability to apply knowledge of mathematics, science, and engineering
b) An ability to design and conduct experiments, as well as to analyze and interpret data
c) An ability to design a hardware and software system, component, or process to meet desired needs within realistic constraints such as economic, environmental, social, political, ethical, health and safety, manufacturability, and sustainability
d) An ability to function on multidisciplinary teams
e) An ability to identify, formulate, and solve engineering problems
f) An understanding of professional and ethical responsibility
g) An ability to communicate effectively
h) The broad education necessary to understand the impact of engineering solutions in a global, economic, environmental, and societal context
i) A recognition of the need for, and an ability to engage in life-long learning
j) A knowledge of contemporary issues
k) An ability to use the techniques, skills, and modern engineering tools necessary for engineering practice.

Program Educational Objectives

PEO1: PREPARATION
Electronics Engineering graduates are provided with a strong foundation to passionately apply the fundamental principles of mathematics, science, and engineering knowledge to solve technical problems and also to combine fundamental knowledge of engineering principles with modern techniques to solve realistic, unstructured problems that arise in the field of Engineering and non-engineering efficiently and cost effectively.

PEO2: CORE COMPETENCE
Electronics engineering graduates have proficiency to enhance the skills and experience to apply their engineering knowledge, critical thinking and problem solving abilities in professional engineering practice for a wide variety of technical applications, including the design and usage of modern tools for improvement in the field of Electronics and Communication Engineering.

PEO3: PROFESSIONALISM Electronics Engineering Graduates will be expected to pursue life-long learning by successfully participating in post graduate or any other professional program for continuous improvement which is a requisite for a successful engineer to become a leader in the work force or educational sector.

PEO4: SKILL
Electronics Engineering Graduates will become skilled in soft skills such as proficiency in many languages, technical communication, verbal, logical, analytical, comprehension, team building, interpersonal relationship, group discussion and leadership ability to become a better professional.

PEO5: ETHICS
Electronics Engineering Graduates are morally boosted to make decisions that are ethical, safe and environmentally-responsible and also to innovate continuously for societal improvement.

Course Teacher	Signature
Dr M.SANGEETHA	
Dr KARTHIK	

Course Coordinator **HOD/ECE**